(12) UK Patent Application (19) GB (11) 2 038 101 A

(21) Application No 7849056
(22) Date of filing
19 Dec 1978
(43) Application published
16 Jul 1980
(51) INT CL³ H05K 3/12
(52) Domestic classification
H1R 10 14 AF
(56) Documents cited
GB 1508560
GB 1316610
GB 1221351
GB 1175832
GB 1145578
GB 1075007
(58) Field of search
H1R
(71) Applicant
Standard Telephones and Cables Limited
190 Strand
London WC2
England
(72) Inventors
Thomas Meirion Jackson
Robert James Hodges
Geoffrey Laurence Ashcroft
(74) Agents
Mr S R Capsey

(54) Printed circuits

(57) A method of fabricating printed circuit devices comprising the steps of depositing a pattern onto an insulating substrate, said pattern being formed of a silver loaded epoxy resin material, immersing the patterned substrate in an electroless copper plating bath and subsequently treating the plated substrate to consolidate the copper plated pattern thereon. Preferably the epoxy resin material is a bisphenol A resin with an aromatic hardener loaded with silver flake particles of 20–50 μm size. Such a resin material can be prepared in a consistency suitable for a silk screen printing process.

GB 2038 101 A

SPECIFICATION

Printed circuits

This invention relates to the fabrication of printed circuit boards.

Existing methods for the production of circuit boards are usually of fully subtractive nature, or based on semi-additive techniques. PCB's made by the subtractive method involves the following processes:

1. Coating of a suitable high grade laminate with copper foil (25–35 μm thick) by adhesive/pressure bonding.
2. Photolithographically defining a circuit pattern in an overlaid etch resist.
3. Wet chemical etching of the exposed copper foil.
4. Stripping of the etch-resist to expose the remaining Cu for further processing e.g. tinning and component insertion. Holes (if required) would be electrolessly plated at this stage.

Semi additive PCB production involves a slightly different approach to that above. Predrilled unclad boards are treated with Sn/Pd ionic solutions to render their surfaces active for electroless Cu plating. The necessary process stages would be:–

1. Clean and prepare the high grade (drilled) laminate.
2. Immerse in $SnCl_2/PdCl_2$ solutions; rinse and dry.
3. Immerse in electroless plating solution plate whole board to thickness of 0.5–1μm (including holes).
4. Apply etch resist pattern.
5. Immerse whole in electroplating bath. Plating exposed areas to 25–35 μm.
6. Remove resist. Immerse in copper etchant and etch away the now exposed thin copper to define discrete conductor areas.
7. Bake to consolidate plating.
8. Tinning and component insertion.

Plating of holes would take place simultaneously with the plating of the flat conductor areas. Fully additive PCB manufacture would use the electroless copper process to deposit all the required copper in the circuit. Methods for defining the conducting areas in electroless plating are several, see for example British Patent 1 487 227. This uses TiO_2 loaded board to replace the Sn^{2+} ions as the electro less plating sensitizer, Pd^{2+} reduction is then achieved only in areas exposed to UV radiation (through a UV mask).

According to the present invention there is provided a method of fabricating printed circuit devices comprising the steps of depositing a pattern onto an insulating substrate, said pattern being formed of a silver loaded epoxy resin material, immersing the patterned substrat in an el ctr less copp r plating bath and subsequently tr ating the plate substrate to consolidate th copper plated pattern thereon.

Embodiments of the inv ntion will now be described. The invention uses metallic silv r as a nucleating medium to promote electroless Cu deposition, where the silver is in the form of fine flake, typically 20–50 μm particle siz ; loaded into an epoxy resin (typically a bis phenol A resin with an aromatic amine hardener). The silver loaded resin is screen printed onto any desired substrate in the desired conductor pattern. If "through board" connections are required e.g. for double sided boards, the holes must be drilled prior to the printing operation. By careful control of the resin rheology and correct choice of printing conditions (e.g. print velocity, screen type, emulsion geometry and substrate to screen separation) it is possible to deposit the loaded resin onto the inside walls of holes contained on the board. A multiple wet-pass technique is used whereby on the first pass the resin is forced through the screen and defines th conductor areas; on the second and subsequent passes the resin will be forced through the screen only in those areas unsupported by the substrate beneath i.e. holes in the substrate. Material is transferred into the hol s and thereby coats the walls. On printing the pattern on the opposite side of the board material will again be deposited at or in hole areas, forming a continuous film between opposite sides of the board. The substrate may be of any material capable of being form d into flat sheet, and capable of withstanding the curing cycle of the conducting resin.

(Before printing on the reverse side of a board the first side must be dried to avoid smudging etc. of the conductor). It is necessary that the printed layer contains metallic silver at the surface, but not that the resin be formulated specifically for low bulk resistivity, since it is the surface properties of the resin that are most important.

The board and conductor are now immersed in an electroless copper plating bath, the formulation of which is well documented and available commercially. Plating commences at 20–22°C, with a maximum plating rate at 35°C; plating rates vary from 0.05 μm per hour, to several microns per hour depending on plating conditions. The rate may be increased by including one or all of the foll w ing treatments to board and plating solution:–

1. Immerse the printed board in an epoxy solvent, dimethyl formamide, methylene dichloride are two (the former being preferred) for 25–30 minutes at room temperature. Dry the board, rinse in deionized water and dry again. Immerse the treated board in th standard electroless copper plating s luti n for 1 to 10 hours (dep nding n th thickness of film r quired). Rinse th plated board, dry and bake at 100–140°C for

1–4 hours to consolidate the Cu plating.

2. Immers the printed board in an epoxy solvent e.g. dimethyl formamide for 5–10 minutes, rinse and dry. To the copper plating solution add 0.05 to 0.1 volume % of 0.5 molar acid tin (2) chloride solution. Immerse the treated board in the prepared solution for 1–5 hours depending on film thickness. Rinse in cold water, dry at 100–140°C for 1–4 hours.

3. Immerse the printed board in a 0.2 molar $SnCl_2$ acid solution for 30″–1′. Rinse in deionized water. Immerse board in standard electroless copper plating solution for 1–5 hours. Rinse and bake 100–140°C for 1–4 hours.

Agitation of the copper plating solution with a low pressure air stream will help to stabilize the solution and aid the wall plating in drilled holes. For optimum results the boards themselves should be gently agitated during the plating period to prevent localized solution depletion. Plating to a thickness of 15–20 μm is possible, above this the plating tends to become non uniform with a flaky, loosely adherent top coat resulting. This must be avoided since the presence of loosely bound copper particles will cause "seeding" and uncontrolled copper deposition on non activated areas of the substrate.

The copper track and plated through holes as prepared above are solderable using standard tin-lead solders, with typical pull-off strengths 140–170 gm mm^{-2} after a 3 second solder run.

Solder times up to 10 seconds have been used with pull-off strengths remaining at or near the average value. Failure of a soldered area takes place within the bulk of the conducting resin film, and not at the substrate-silver resin, resin-copper, or copper-solder interfaces.

The size of the substrates or printed geometrics is only limited by the conducting resin printing methods. It is possible to (electroless) copper plat silver loaded resin tracks of any size, at least down to (and including) 0.25 mm track width. No acid etches are required to prepare or pre-treat the boards.

The invention allows conducting track to be deposited onto a variety of substrates and provides a means of achieving through board connections between selected areas on either sid of the substrate, and also a means wher by discrete components may be inserted into the board and connected to the conducting areas by means of soldering. The method also allows the integration of printed compon nts such as switches and terminati ns suitable for use with sprung edge c nnectors.

CLAIMS

1. A method of fabricating printed circuit devices comprising the steps of depositing a pattern onto an insulating substrate said pattern being formed of a silver loaded epoxy resin material, immersing the patterned substrate in an electroless copper plating bath and subswquently treating the plated substrate to consolidate the copper plated pattern thereon.

2. A method according to claim 1 wherein the expoxy resin material is a bisphenol A resin with an aromatic amine hardener.

3. A method according to claim 1 or 2 wherein the silver is in flake form of 20–50 μm particle size.

4. A method according to any preceding claim wherein the silver loaded epoxy resin material is deposited by a silk screen printing process.

5. A method according to claim 4 wherein the substrate is a sheet or board having holes therethrough, in areas covered by the pattern, the pattern being screen printed a first time to deposit the epoxy resin material onto the substrate face and a second time to deposit the epoxy resin material onto the inside walls of the holes.

6. A method according to any preceding claim wherein the substrate is a sheet or board and a pattern is deposited on both faces thereof.

7. A method according to any preceding claim including the step of immersing the substrate bearing the printed pattern for a predetermined period of time in an epoxy solvent and then rinsing the substrate prior to immersing the substrate in the electroless copper plating bath.

8. A method according to any preceding claim including the step of immersing the substrate bearing the printed pattern for a predetermined period of time in a 0.2 to 0.5 molar $SnCl_2$ acid solution and then rinsing th substrate prior to immersing the substrate in the electroless copper plating bath.

9. A method according to any preceding claim wherein the consolidation treatment comprises baking the substrate at a temperature of between 100°C and 140°C.

10. A method of fabricating printed circuit devices substantially as described.

11. A printed circuit device fabricated by the method of any preceding claim.

Printed for Her Majesty's Stationery Office
by Burgess & Son (Abingdon) Ltd.—1980.
Published at The Patent Office, 25 Southampton Buildings,
London, WC2A 1AY, from which copies may be obtained.